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Implementation of five-stage CS-VCO circuit on 250nm CMOS Technology for Low Power Digital Applications

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Abstract: **This paper presents a low power, low cost design of PLL (Phase Locked Loop).The proposed PLL comprises of PFD(Phase frequency Detector),CP(Charge Pump), Second order low pass filter as a loop filter and CS-VCO(Current starved- Voltage control Oscillator). The VCO used for the designed. PLL shows higher tuning range i.e. 156MHz- 169.73MHz with low power consumption of 5.55mW, also it is designed such that, it eliminate the function of frequency divider circuit to some extent . The proposed PLL circuit is designed and simulated on Generic 250nm CMOS technology.**

Keywords: **PLL, PFD, CP, VCO, CS-VCO, CMOS, Power consumption.**

I. INTRODUCTION

PLL plays a major role in all modem digital communication Systems, wired and wireless systems. In the design of PLL, VCO is a crucial building block. Any jitter, spur or power consumption generated at the output of PLL due to digital blocks is the main source to degrade the system performance [7], [8], [9]. Many researches has been done to improve the performance of PLL in the last few decades which results power reduction of circuit by eliminating the frequency divider circuit, with the context of improvisation in other factors like jitter, frequency range, noise reduction at low voltage supply while getting numerous applications in frequency synthesizer, Zigbee applications and IoT(Internet of things) by modifying the internal circuitry. Conventionally PLL systems have been tested based on its circuit functionality and functional specifications is verified at some pre-specified test points. This rising popularity is providing strong motivation in finding a low-cost 5- stage CS-VCO based PLL. In previous work [1],[2] and [3], the PLL was designed without using frequency divider circuit on its feedback from VCO to PFD with some modifications obtaining High VCO gain, larger tuning range of VCO, greater lock range with low power dissipation and lees jitter as compared to the previous work. In this paper, Section-1 has the Introduction part, Section-2 represents the proposed methodology with circuit description, Section-3 shows the transient and power analysis with its simulation waveforms, Section- 4 discusses its result and compares with previous work done and Section- 5concludes the proposed work.

II. PROPOSED METHODOLOGY

The paper is mainly focusing on the VCO design with less circuit complexity by elimination of frequency divider circuit and increased tuning frequency range which is achieved through proper sizing of five-stage CS-VCO. The power dissipation performance for the whole PLL circuit is evaluated and simulated for the optimal circuit performance. The proposed PLL designed is shown in below figure.

PLL can be designed in many ways depending upon the requirement of outputs its internal circuitry has been modified.

A. PFD

The PFD receives and compares the phase and frequency of output coming from VCO with the external input or reference signal and generates corresponding variable output voltage UP or DOWN as per the phase difference (also known as phase error) UP signal will goes HIGH if the phase difference follows VCO frequency else DOWN signal will be HIGH and its output is fed to charge pump. In the next section we discuss about charge pump.

The voltage source transistors MP1 and MP2, voltage switches transistor MN1, MN2, MN6 and MN7 and current mirror transistors are MN20, MP40 and MP8 with no dummy transistors present in this circuitry. The output of PFD has given as input to the charge pump, named CP_i1 and CP_i2.

B. Charge Pump

A charge pump is alike DC to DC converter for energetic charge storage to increase or decrease voltage by using capacitors. In each cycle, the time during which the switch is turned on is proportional to the phase error. In PLL a charge pump is basically a bipolar switched current source i.e. it can give positive or negative current pulses as output into the loop filters. It is used to transmit digital signal from phase frequency detector to an analog signal for controlling the voltage-controlled oscillator which is leaded by output signal of CP. The output voltage of the CP must be kept constant

The proposed charge pump implementation circuit is shown in above Fig 4.2 the circuit shown consists of UP and DN switches like MP1 and MN1, current source transistors MN3 and MP2, a variable current reference providing current Icp and current mirrors are MN2, MP7 and MP8. MN1, MN7 MN9 and MP3 are dummy transistors used to match with switches (voltage drop).

C. Loop Filter

In this thesis second order loop filter has shown in below Fig. 4.3 in the proposed circuitry the value of capacitor C1 is 5times more than the capacitor C2 having range in pico farads and resistor in mega ohms. The generated voltage output of loop filter is further given as input to the VCO to control the output frequency.

D. VCO

A VCO circuit is actually a ring oscillator, the gain stages are connected in a loop, whose output is given to a first stage. The circuit must satisfy the barkhausen criteria for sustained oscillation, where it must have a phase shift of 360 degree. The DC inversion provides 180 degree phase shift and remaining has been equally divided among all the stages of ring oscillator, so each delay gives 180/N of phase delay, where N- is no. of stages in oscillator

Fig 4 below shows the schematic diagram of VCO (Voltage Controlled Oscillator). In the proposed schematic the transistors MN13 and MP2 works as current limiter for inverter (MN1 and MP8). Similarly, six such arrangement are connected in series have introduced in this design which gives sinusoidal output and last inverter (MN7 and MP14) is used for inversion into sinusoidal waveform.

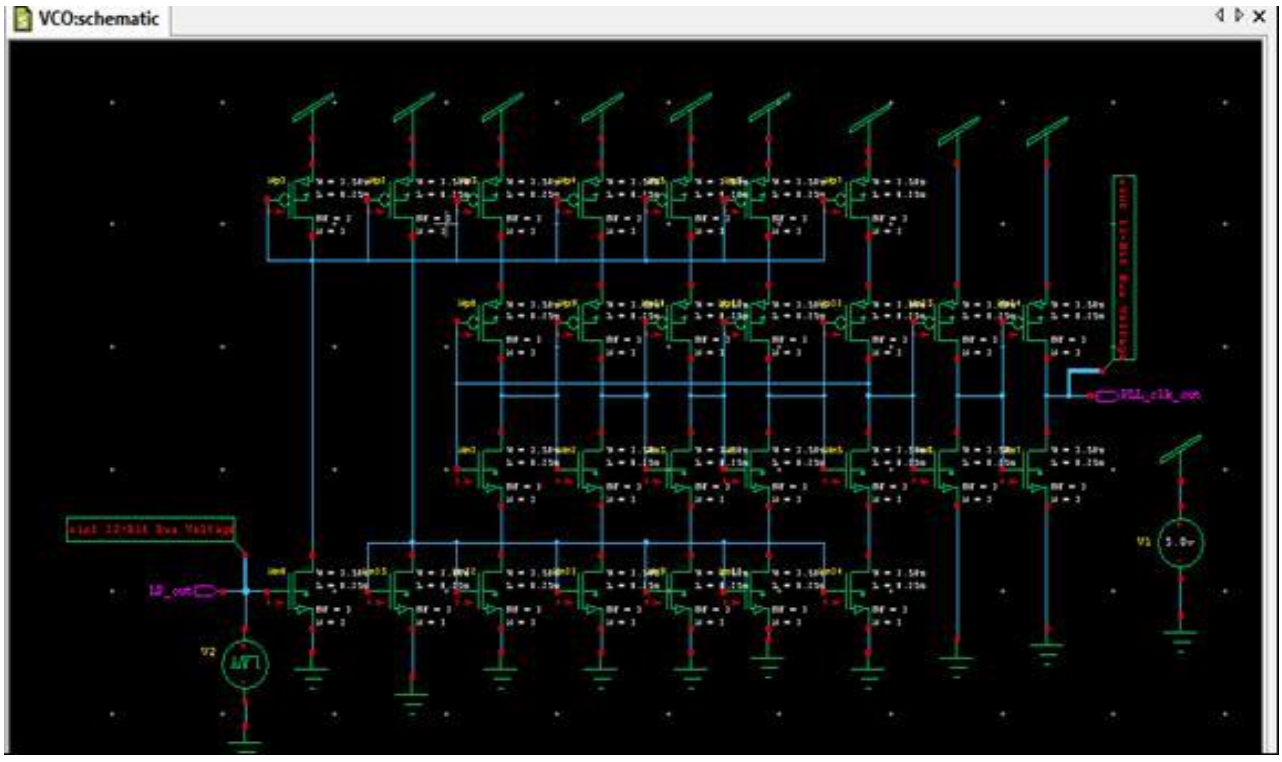

Fig 1: VCO Schematic

III. SIMULATION RESULT

Two pulse signals of different frequencies are connected to the inputs of Phase Frequency Detector, and resulted signal (UP/DOWN) is observed at output terminals of PFD.

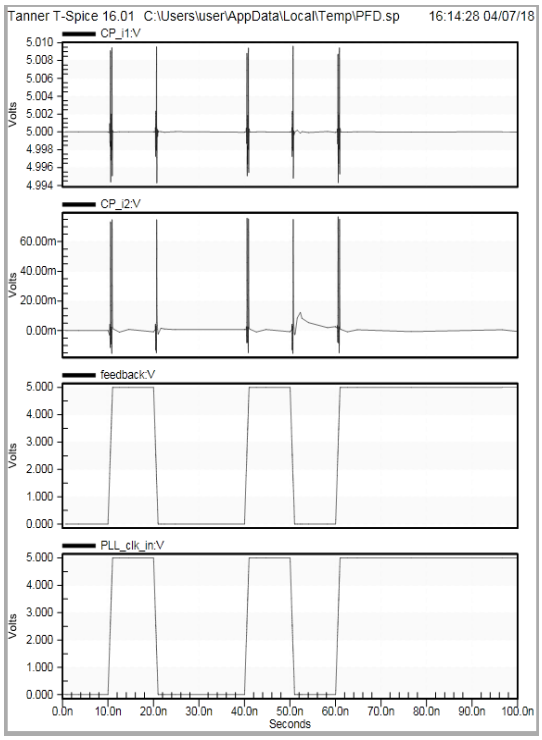

Fig 2: Transient response of PFD

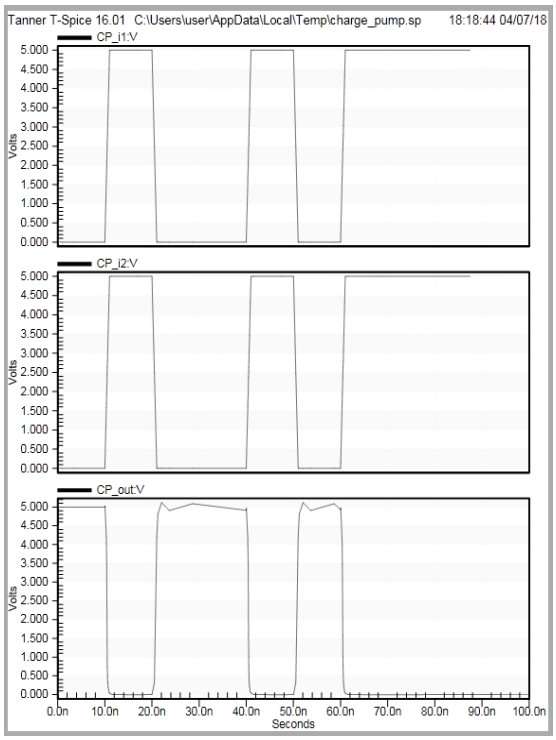

Fig 3: Transient analysis of charge pump

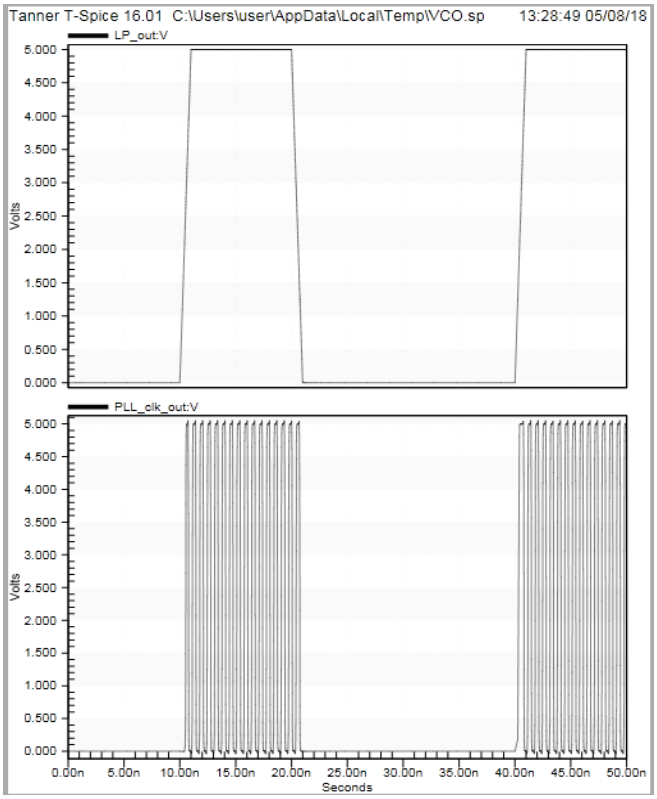

Fig 4: Transient response of CS-VCO

A ramp signal (0.0 V-1.8 V) is connected to the input of VCO as control voltage and corresponding oscillation frequency is observed at VCO output terminal.

IV. RESULT AND DISCUSSION

The comparison of different modified PLL architectures is reported in Table-I which shows the various comparative results to the previous done works. In this the various parameters are extracted in different CMOS technologies. As compare to the previous results, this work successfully able to achieve low power consumption and also achieved good tuning range and VCO gain.

TABLE I: COMPARISON WITH PREVIOUS WORK

Ref .no	Supply Voltage (V)	Tuning Range (MHz)	VCO Gain (GHz/V)	Jitter (ps)	Technology (CMOS nm)	Power (mW)
[2]	1.8	431-1796	1.48	-	180	7.08
[3]	1.8	500-1500	-	24	180	.32
[1]	1.8	167-1711	2.21	9.8	180	0.27
[37]	1.8	320-960	-	-	180	20
[38]	1.2	1000-1500	1.72	-	130	25
[39]	1.8	320-960	9.31	-	180	20
This work	1.8	155-1271	1.45	11.2	250	5.55

V. CONCLUSION

In designing an IC there are two important factors which should be considered for better performance of IC's i.e. power consumption and speed. Right here in this work power consumption is the main base for doing this project. A PLL designed by means of built-in CMOS has executed the fine importance within the last few many years considering the fact that of the high performance system design within the digital and communication area. This work presents transistor level circuit design and output simulation of PLL using five-stage CS-VCO along with its various components like PFD, CP and Loop filter. CMOS technology has chosen due to its advantages of low power consumption and smaller layout area can be achieved and also noise has reduced.

In the proposed work a 5-stage ring oscillator has been modified and implemented in replacement of frequency divider circuit which was connected in feedback from VCO to PFD. Following conclusions have been drawn from this work. Circuit complexity has been reduced by removal of frequency divider circuit from feedback of PLL. Low power consumption has achieved. Size of chip has also minimized to some extent. Output is nearly similar to that of source project but not exactly same. After combining all the basic components of PLL in the proposed order, it has been calculated an average power consumption of PLL is 5.55mW, with a voltage supply of 1.8V with large tuning range(155MHz-1.271GHz), high gain(1.45GHz/V) and max jitter 11.2ps. It is simulated in T-SPICE simulator of Mentor Graphic Tanner EDA 16.3 Tool.

REFERENCES

[1] Anshul Agrawal, Rajesh Khatri "Design of Low Power, High Gain PLL using CS-VCO on 180nm Technology" International Journal of Computer Applications (0975 – 8887) Volume 122 – No.18, July 2015.

[2] Ashish Mishra, Mr. Gaurav Kr. Sharma Dr. D. Boolchandani" Performance Analysis of Power Optimal PLL Design Using Five-Stage CS-VCO in 180nm" International Conference on Signal Propagation and Computer Technology (ICSPCT) 2014 IEEE

[3] S. Moorthi, S. Aditya" A Low Jitter Wide Tuning range Phase Locked Loop with Low Power Consumption in 180nm CMOS Technology" 2013 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia).

[4] Mrs. Devendra Rani and Prof.SanjeevM.Ranjan,"A Voltage Controlled Oscillator Using Ring Structure In CMOS Technology",International Journal Of Electronics And Computer Science Engineering Vol.1,No.3,ISSN 2277-1956.

[5] FahmidaKhatoon, Tarana A chandel "DESIGN OF RING VCO USING NINE STAGES OF DIFFERENTIAL AMPLIFIER" IJRET: International Journal of Research in Engineering and Technology eISSN: 2319-1163 | pISSN: 2321-7308.

[6] Yonghui Tang, Randall L. Geiger "A 2.5GBIT/S CMOS PLL FOR DATA/CLOCK RECOVERY WITHOUT FREQUENCY DIVIDER" this work is supported in part by National Semiconductor Inc. and the R. J. Carver trust.

[7] A.A. Abidi, F. Behbahani, and A. Kral, "RF-CMOS oscillators with switched tuning,"In Proc, IEEE Custom Integrated circuits Conf, 1998,pp. 555-558.

[8] B.Razavi, "Design of Analog CMOS Integrated Circuits," Tata McGraw Hill Edition,200 1.

[9] Chi-Wa Lo and H.C. Luong, " A 1.5-V 900-MHz monolithic CMOS fast switching frequency synthesizerfor wireless applications," IEEE J. Solid-State Circuits,vol.37, no.4, pp. 459-470, April 2002.

[10] S. Verma, J. Xu, T. H. Lee, "A Multiply-by-3 Coupled Ring Oscillator for Low power Frequency Synthesis," IEEE J. Solid State Circuits, vol. 39, pp. 709-713 , Apr., 2004.

[11] Kim, Seung-Hoon, and Sang-bock Cho. "Low phase noise and Fast locking PLL Frequency Synthesizer for a 915MHz ISM Band." In Integrated Circuits, 2007. ISIC07. International Symposium on, pp. 592-595. IEEE, 2007.

[12] Liu, Huihua. "Design of low phase noise and fast locking PLL frequency synthesizer." In 2011 International Conference on Electric Information and Control Engineering, pp. 4113-4116. 20 II.